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A DSOGI-FLL-based Dead-Time Elimination PWM for Three-Phase Power Converters

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***Abstract*—The dead-time elimination pulse width modulation (PWM) enables the drive pulses of the upper and the lower switching devices to alternate according to the current polarity, thus abandoning the dead-time and essentially avoiding the dead-time effect in power converters. However, the current zero-crossing will be distorted by the current jump generated by the drive-pulse alternation. And the current zero-crossing distortion will be further intensified if errors exist in the detected current polarity. Thanks to the noise-attenuation and frequency-adaptability characteristics of the double second-order generalized integrator frequency-locked loop (DSOGI-FLL), it can obtain accurate current polarities even in harmonic and unbalanced conditions. A DSOGI-FLL-based dead-time elimination PWM is therefore proposed in this paper, and several improvements are made to minimize the current zero-crossing distortion. An underlap period is added when alternating the upper and lower drive pluses to smooth the current jump at zero-crossing. And a delay compensation term is inserted in the DSOGI-FLL to compensate both the current measurement delay and the control delay. The effectiveness of the proposed DSOGI-FLL-based dead-time elimination PWM has been validated by experiments respectively in the unbalanced-current, power-change, and frequency-variation conditions with a *RL* load, as well as in a grid-connected converter.**

***Index Terms*—Dead-time elimination PWM, DSOGI-FLL, zero-crossing distortion, delay compensation, power converters.**

I. Introduction

The two-level voltage-source power converter has already been widely used for a long time in various areas, e.g. renewable power generation systems, motor drive systems, active power filters, etc. However, the dead-time effect with the conventional pulse width modulation (PWM) is always an accompanied issue in the application of the converter, which can cause voltage losses, generate low-frequency (mainly 5^{th} and 7^{th}) voltage/current harmonics, and reduce the dc-link voltage utilization [1]. The dead-time effect is especially serious in the low-speed motor drive system [2] and the high-switching frequency converter [3], [4], where large numbers of dead-time voltage errors are included in a fundamental period. Specifically, with nowadays developed wide-bandgap devices, the switching frequency of converters can reach up to 100kHz (with silicon carbide devices [4]), or even several MHz (with gallium nitride devices [5]). The dead-time effect will be further intensified with the ultra-high switching frequency and must be well addressed.

Numerous dead-time compensation schemes have been proposed [6]-[10]. Given the voltage error generated by dead-time is related to the current polarity, most of the well-known dead-time compensation methods are implemented by adjusting the amplitude of the modulation wave according to the current polarity [6], [7]. The performance of the dead-time compensation therefore highly relies on the accuracy of the current-polarity detection. Apart from the dead-time compensation methods which directly adjust the amplitude of the modulation wave according to the current polarity, there are also many other methods, e.g. the current-detection-independent dead-time compensation method based on terminal voltage A/D conversion [8], the adaptive feed-forward dead-time compensation [9], the dead-time compensation using the integrator output of the synchronous d-axis current PI controller [1], etc. In addition, to compensate the low-frequency current harmonics caused by the dead-time effect, the proportional-resonant (PR) controller and the repetitive controller, which have high gains at harmonic frequencies, can be employed for dead-time compensation [10]. However, the existing dead-time compensation schemes are just remedies for the dead-time effect of the conventional PWM, which are impossible to precisely and thoroughly eliminate the dead-time effect.

Rather than using the conventional PWM with dead-time compensation, the dead-time elimination PWM [11], [12] can also be adopted, which alternately generates the upper and the lower drive pulses according to the current polarity. Due to the abandon of dead-time, the dead-time elimination PWM can essentially avoid the dead-time effect and reduce the possibility of the shoot-through failure [13]. However, the requirement of current polarity detection complicates the control of the dead-time elimination PWM, and the current zero-crossing will be distorted by the current jump generated by the drive-pulse alternation [14] and additionally intensified if errors exist in the detected current polarity, which are important factors of limiting the wide-spread application of the dead-time elimination PWM.

Several strategies have been proposed for the control of dead-time elimination PWM and the minimization of current zero-crossing distortions [11]-[18]. The accuracy of the current-polarity measurement was enhanced in [11] and [12] by detecting the conduction of switching devices with auxiliary circuits. However, the complexity of the converter circuit is increased with an additional electrical-isolation problem. In [14], a strategy combining the phase-shift control and the dead-time elimination PWM is applied to the cascade dual-buck inverter with reduced current ripple and minimized zero-

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crossing distortion. But the combining strategy is not applicable to converters of other topologies. In [15] and [16], the dead-time elimination PWM was implemented with the current hysteresis control strategy, and the high switching frequency adopted at the current zero-crossing may reduce the current ripple and minimize the distortion. However, it is inevitable to encounter the drawback of the hysteresis control with variable switching frequencies, i.e., the large bandwidth of the generated current harmonics makes the filter design challenging. In closed-loop systems, the current reference with good immunity to noise and no ripple at zero-crossing can also be used to implement the dead-time elimination PWM [13]. A drawback is that, the control error between the current reference and the real output current may cause serious current zero-crossing distortions. In [17], a fundamental period of the current is divided into the nonzero-crossing zone and the zero-crossing zone, where the dead-time elimination PWM and the conventional PWM are respectively applied, so that the accuracy requirement of the current-polarity detection can be reduced. Similarly, an immune-algorithm-based dead-time elimination scheme was proposed in [18] for the single-phase inverter, and applying different schemes in nonzero-crossing and zero-crossing zones. However, the scheme is not a real dead-time elimination PWM due to the dead-time still exists in the zero-crossing zone, and extra current distortions can be generated when different schemes switch between nonzero-crossing and zero-crossing zones.

This paper therefore aims to propose a practical control strategy for the dead-time elimination PWM with minimized current zero-crossing distortion to essentially solve the dead-time effect in power converters. Thanks to the noise-attenuation and frequency-adaptability characteristics of the second-order generalized integrator frequency-locked loop (SOGI-FLL) [19]-[22], it is suitable to obtain accurate current polarities to implement the dead-time elimination PWM. And considering the unbalanced condition where the phase difference of three-phase currents is not evenly equal to $2\pi/3$, the double second-order generalized integrator frequency-locked loop (DSOGI-FLL) [23]-[25] is adopted, which can extract both the positive- and negative-sequence current components. The DSOGI-FLL and the dead-time elimination PWM are innovatively integrated in this paper by proposing a DSOGI-FLL-based dead-time elimination PWM. And several improvements are further made to minimize the current zero-crossing distortion, including an underlap period added in the drive pulses to smooth the current jump, and the delay-compensation term inserted in the DSOGI-FLL to compensate both the current measurement delay and the control delay.

Since delays (e.g. control and measurement delays) in the digital-control system can seriously deteriorate the performance of converters, numerous researches have been reported in the compensation of delays. Various delay-compensation methods have been proposed for enhancing the damping ability of *LCL* filters [26], [27], improving the stability and dynamic performance of converters [28]-[30], suppressing output current harmonics [31]-[33], etc. The linear prediction is implemented by the iteration algorithm using consecutive history samples [28]. Though characterized by a significantly-low computation burden and independent of plant models, the linear prediction has a poor accuracy for delay compensation. The Smith predictor [28], the current observer [32], [34] and the model predictive control [33] can ideally completely compensate the delay in control systems, which however require precise plant models and are thus sensitive to plant parameters. Phase-lead compensators [27], [29], [30] can be used to compensate the delay of a certain-frequency component. However, the phases of other-frequency components will also be influenced to different degrees, presenting a nonlinear-compensation characteristic for signals containing components of different frequencies. The repetitive predictor is effective for compensating the delay in periodic signals [26], [31] while has drawbacks of high frequency-variation sensitivity and low dynamic response. The DSOGI-FLL adopted in this paper has noise-attenuation and frequency-adaptability characteristics, as well as the ability of extracting both the positive- and negative-sequence components, which can work well for detecting current polarities even in harmonic and unbalanced conditions. And the delay compensation implemented with the DSOGI-FLL is specially designed to compensate the current-polarity error caused by control and measurement delays, so that accurate current polarities can be obtained for implementing the dead-time elimination PWM with minimized current zero-crossing distortions. In contrast, the above reviewed delay-compensation methods cannot fully meet the requirements of noise-attenuation, frequency-adaptability, and applicability in harmonic and unbalanced conditions, which are not preferred in the current-polarity detection for the dead-time elimination PWM.

The main contribution of this paper lies in the proposed DSOGI-FLL-based control strategy for solving the control and current zero-crossing distortion issues in the dead-time elimination PWM. With a delay-compensation term inserted in the DSOGI-FLL and an underlap period added when alternating the upper and the lower drive pluses, the DSOGI-FLL-based dead-time elimination PWM enables the converter to work well in harmonic and unbalanced current conditions with minimized current zero-crossing distortion. The authors hope the proposed strategy can promote the wide application of the dead-time elimination PWM to thoroughly solve the dead-time effect in power converters, which can be beneficial not only to the operation of the conventional power converter with silicon IGBTs, but also to the ultra-high switching-frequency converter with new-emerging wide-bandgap devices.

The remaining parts of this paper are structured as follows. Section II presents the modulation mechanism of the dead-time elimination PWM and the current zero-crossing distortion issue. In Section III, an underlap period is inserted when alternating the upper and the lower drive pulses to smooth the current jump at zero-crossing. The SOGI-FLL is presented and modified with the delay compensation in Section IV. The DSOGI-FLL-based dead-time elimination PWM is proposed in Section V and applied to the grid-connected converter in Section VI. Lastly in Section VII, the effectiveness of the DSOGI-FLL-based dead-time elimination PWM is validated by experiments respectively with a *RL* load and in the grid-connected condition.

II. Modulation Mechanism and Issues of the Dead-time Elimination PWM

A. Modulation Mechanism of the Dead-Time Elimination PWM

The modulation mechanism of the dead-time elimination PWM in Phase A is presented in Fig. 1, where S_a^+ and S_a^- are the upper and the lower drive pulses; u_a^* is the modulation wave; i_a^* is the detected reference current providing the current polarity information. As seen, the drive pulse in half the

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fundamental period is disabled according to the detected current direction. During the period when both S_a^+ and S_a^- are low, the output voltage is generated by the current freewheeling through the body diode, to guarantee the principle of equivalent accumulated impulse.

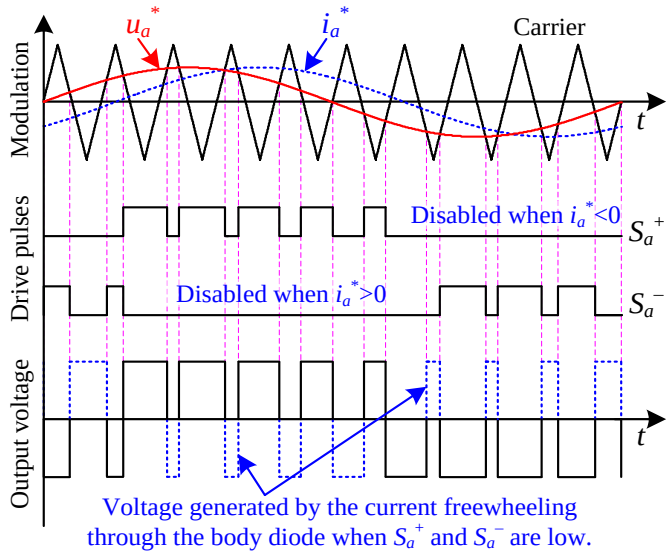

Fig. 1. Modulation mechanism of the dead-time elimination PWM in Phase A.

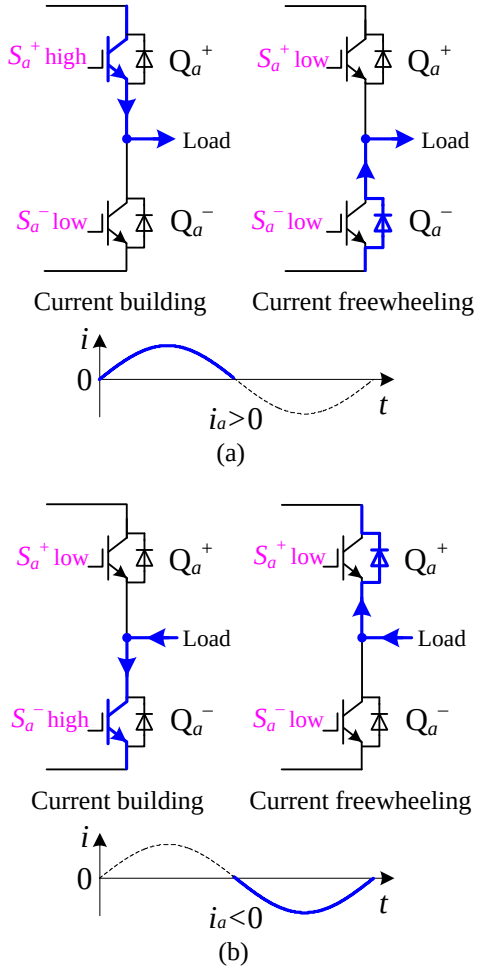

Fig. 2. Current paths with the dead-time elimination PWM: (a) current building and freewheeling stages when i_a<0 and (b) current building and freewheeling stages when i_a>0.

The detailed current paths in Phase A with the dead-time elimination PWM is illustrated in Fig. 2, where Q_a^+ and Q_a^- are the upper and the lower switching devices, respectively. In a switching period, the current building stage and the current freewheeling stage can be divided according to the state of the switching devices. Taking i_a>0 in Fig. 2(a) for example, in the current building stage when S_a^+ is high and S_a^- is low, the channel of Q_a^+ will turn on actively building the output current; in the current freewheeling stage where both S_a^+ and S_a^- are low, the current will be freewheeled by the body diode of Q_a^-. Conversely when i_a<0 in Fig. 2(b), the channel of Q_a^- and the body diode of Q_a^+ will alternately endure the building current and the freewheeling current.

No dead-time is required in the dead-time elimination PWM. Consequently, the output voltage/current will not be distorted by the dead-time voltage errors so that the dead-time effect can be essentially avoided. In addition, the abandon of the dead-time also reduces the possibility of the shoot-through failure [13]. However, the requirement of the current polarity can complicate the implementation of the dead-time elimination PWM and cause the current zero-crossing distortion, which will be analyzed in detail in next section.

B. Current Zero-Crossing Distortion caused by the Current Jump and the Error in the Detected Current Polarity

Two factors can cause the current zero-crossing distortion in the dead-time elimination PWM: one is the current jump when alternating the upper and the lower drive pulses, the other is the error in the detected current polarity.

As presented in Fig. 2, the enabled drive pulse S_a^+ cannot actively make the current decrease and cross the zero line making i_a<0. Therefore, near the current zero-crossing with i_a>0, the current can only fluctuate on the zero line achieving a positive average value. Similarly, near the current zero-crossing with i_a<0, the current can only fluctuate under the zero line achieving a negative average value. Consequently, the current cannot cross the zero line smoothly, and a current jump will be generated, which can be seen in the zoomed-in zero-crossing in Fig. 3.

Apart from the distortion caused by the current jump, if a large error exists in the current polarity given to the dead-time elimination PWM, the current will not cross the zero line in time which will further intensify the current distortions at zero-crossing. As illustrated in Fig. 3, the polarity of the reference current i_a^* is delayed by T_{pd} compared with the real polarity of the output current. Correspondingly, the moment when alternating the drive pulse is also delayed by T_{pd}. As seen the zoomed-in current zero-crossing, after the current reaches the zero line, the upper drive pulse S_a^+ makes the current always fluctuate but cannot cross the zero line, until the drive pulse is switched to S_a^-. Therefore, the delay in current polarity can cause serious distortion at the current zero-crossing. And as seen the three-phase output currents in Fig. 3, the current zero-crossing distortion in one phase can also distort the currents of the other two phases at the same time.

In addition, the current fluctuation around the zero line can indicate that, it is not feasible to simply adopt the detected current polarity of the current switching period to alternate the drive pulses in the next switching period, which can never make the current cross the zero line.

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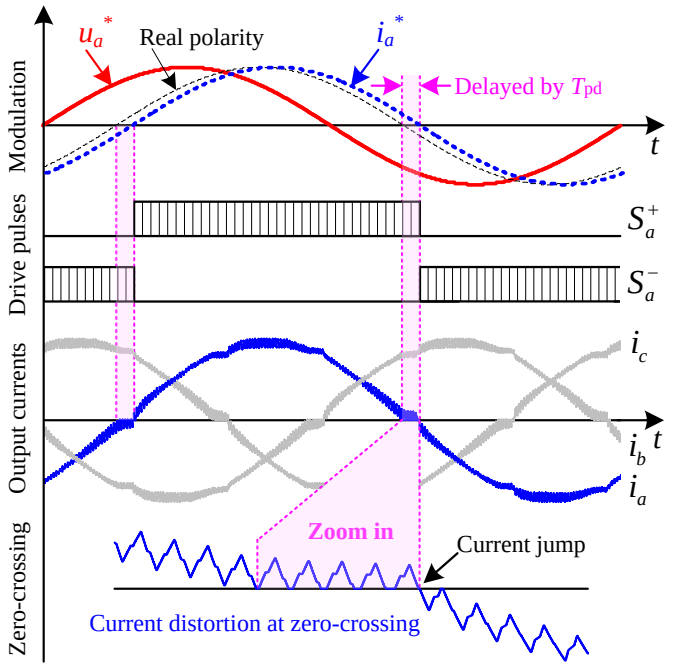

Fig. 3. Dead-time elimination PWM with the current polarity delay.

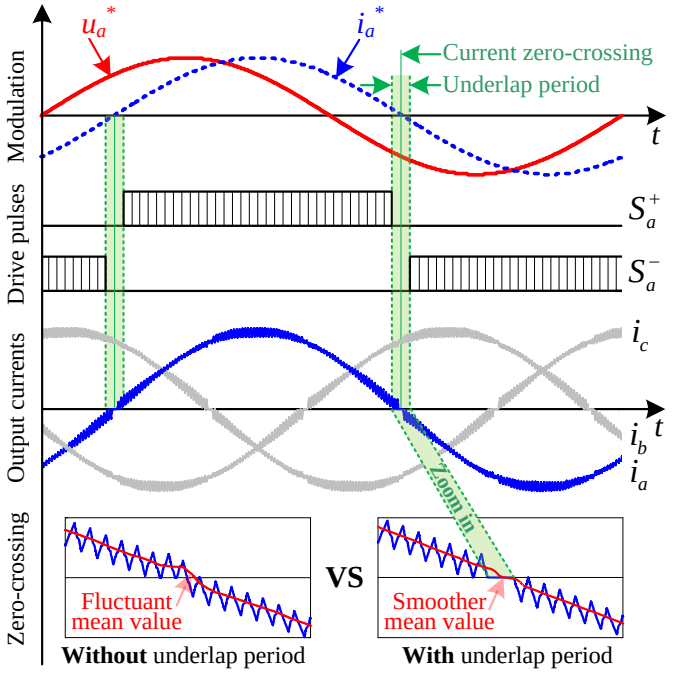

Fig. 4. Dead-time elimination PWM with the underlap period between the upper and the lower drive pulses.

III. Underlap Period between the Upper and the Lower Drive Pulses for Smoothing the Current Jump

To mitigate the zero-crossing distortion caused by the current jump, an underlap period is added between the upper and the lower drive pulses of the dead-time elimination PWM, as shown in Fig. 4. In the underlap period, both the upper and the lower drive pulses are disabled. Note that, the added underlap period is not like the conventional dead time which should be as short as possible. The period is relatively long, e.g. equal to several switching periods, to help the current cross the zero line smoothly.

The improvement of the current distortion can be seen in Fig. 4 by comparing the mean values of the zoomed-in current zero-crossings respectively without and with the underlap period, which are computed over a running average window of one switching cycle. As seen, the mean value with the added underlap period is smoother than that without the underlap period. Furthermore, the corresponding distortions in the other two phase currents can also be simultaneously mitigated. Though the distortion improvement is small, the added underlap period can be necessary due to it does not increase the complexity of the modulation and does help avoiding the shoot-through risk.

Ideally, the underlap period should be decided according to the number of current ripple crossing the zero line, which is influenced by several factors, e.g. the dc-link voltage, the modulation index, the filtering inductance, and the output current amplitude [35], [36]. However, letting the underlap period varies with the operation conditions can complicate the modulation. Considering the distortion improvement by the added underlap period is small and an excessively large underlap period may intensify the current zero-crossing distortion, the underlap period equal to fixed even number (e.g. 2 or 4) switching cycles is suggested.

IV. SOGI-FLL with Delay Compensation

To further minimize the current zero-crossing distortion, besides the added underlap period, the error in the current polarity given to the dead-time elimination PWM should also be minimized. The adaptive filter SOGI-FLL [19]-[22] for obtaining accurate current polarities, as well as the modification for delay compensation, will be presented in this section.

A. Characteristics of SOGI-FLL

The structure of SOGI-FLL is shown in Fig. 5, where ω' and k are the resonance frequency and the damping factor, respectively; ε_i is the signal error between the measured current i_m and the detected fundamental component i'; i' and qi' are two in-quadrature signals.

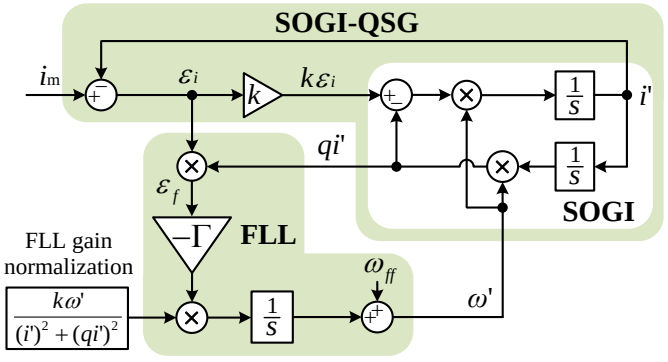

Fig. 5. Structure of SOGI-FLL.

The characteristic transfer functions of SOGI-FLL can be given by (1), (2), and (3). The corresponding responses are plotted in Fig. 6.

$$SOGI(s)=\frac{i'(s)}{k\varepsilon_i(s)}=\frac{\omega's}{s^2+\omega'^2} \tag{1}$$

$$D(s)=\frac{i'(s)}{i_m(s)}=\frac{k\omega's}{s^2+k\omega's+\omega'^2} \tag{2}$$

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$$Q(s)=\frac{qi'(s)}{i_m(s)}=\frac{k\omega'^2}{s^2+k\omega's+\omega'^2} \tag{3}$$

The frequency response of $SOGI(s)$ in Fig. 6 shows that, the SOGI acts as an infinite-gain integrator for the sinusoidal signal with the frequency of ω' (resonant characteristic), and can track the signal with a zero steady-state error [37]. $D(s)$ and $Q(s)$ in Fig. 6 respectively provide the band-pass and low-pass filtering characteristics to i' and qi', which can attenuate harmonics and noise of the measured current i_m [34]. And provided $\omega'=\omega$, qi' in $Q(s)$ will always be $\pi/2$ lagging i' in $D(s)$ independently of ω' and k, verifying that the SOGI-based filtering structure can serve as the quadrature signal generation (QSG). Usually, the damping factor k is selected as $\sqrt{2}$, roughly resulting in an optimal relationship between the settling time and overshooting in the dynamic response [22].

The FLL in Fig. 5 is adopted to make the SOGI become frequency adaptive. According to [25], the frequency error variable ε_f ($\varepsilon_f = \varepsilon_i \cdot qi'$) will be positive when $\omega<\omega'$, zero when $\omega=\omega'$, and negative when $\omega>\omega'$. Therefore, the polarity of ε_f can be used to obtain the direction of tracking the input-signal frequency, which is final realized by an integral controller with a negative gain $-\Gamma$ shifting ω' until $\omega'=\omega$. In addition, the FLL gain is normalized by $(i')^2+(qi')^2$ to linearize the response of the frequency adaptation loop [22]. The additional frequency ω_{ff} is used to accelerate the initial synchronization process.

With the noise-attenuation and frequency-adaptability characteristics, SOGI-FLL can be an ideal algorithm to accurately obtain the current polarity for alternating drive pulses in the dead-time elimination PWM. However, in the digital control system, the current measurement delay T_{md} caused by the conditioning circuit is inevitable, and the alternation command of drive pulses will take effect with a control delay T_{cd} [31], which can together affect the accuracy of the obtained current polarity. Therefore, the conventional SOGI-FLL will be modified with delay compensation in next section.

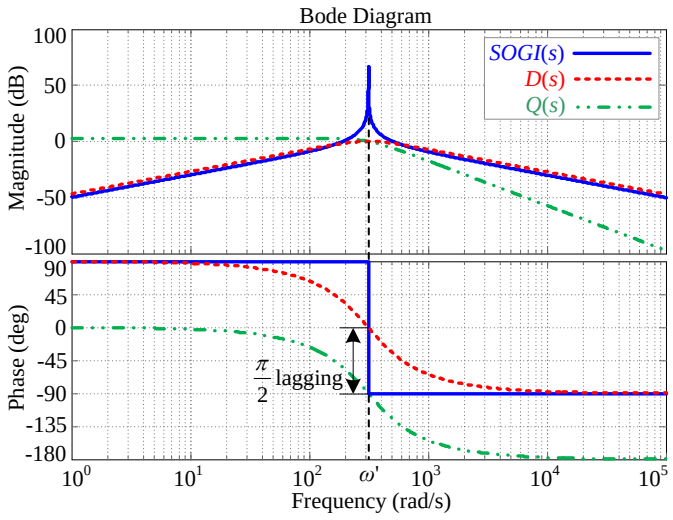

Fig. 6. Frequency responses of $SOGI(s)$, $D(s)$, and $Q(s)$ with $\omega'=100\pi$ and $k=\sqrt{2}$.

B. Modified SOGI-FLL with the Delay Compensation

The modified SOGI-FLL with the delay compensation is shown in Fig. 7, where a first-order inertial term $1/(T_d s+1)$ is inserted between the measured current i_m and the converter output current i, representing both the current measurement delay T_{md} and the control delay T_{cd}, i.e., $T_d = T_{md}+T_{cd}$. To compensate the delay, another first-order inertial term $1/(T_c s+1)$ is added in the feedback loop between i' and i''. The corresponding relationships of the currents in the frequency domain can be expressed as

$$i_m(s)=\frac{1}{T_d s+1}i(s), \tag{4}$$

$$i''(s)=\frac{1}{T_c s+1}i'(s). \tag{5}$$

In the SOGI-FLL control loop, due to the infinite gain of SOGI at the frequency of ω', the error ε_i between the input current i_m and the feedback current i'' will still be zero in steady state. Therefore, the current relation in (2) is still valid and rewritten as

$$D'(s)=\frac{i''(s)}{i_m(s)}=\frac{k\omega's}{s^2+k\omega's+\omega'^2}. \tag{6}$$

Submitting (4) and (5) into (6), the relation between i' and i can be obtained as

$$\frac{i'(s)}{i(s)}=\frac{k\omega's}{s^2+k\omega's+\omega'^2}\cdot\frac{T_c s+1}{T_d s+1}. \tag{7}$$

As seen in (7), if $T_c=T_d$ is selected, the influence of the delay on the current polarity detection can be effectively eliminated. At the frequency of ω', both the magnitude and the phase of the detected current i' will exactly be equal to those of the output current i.

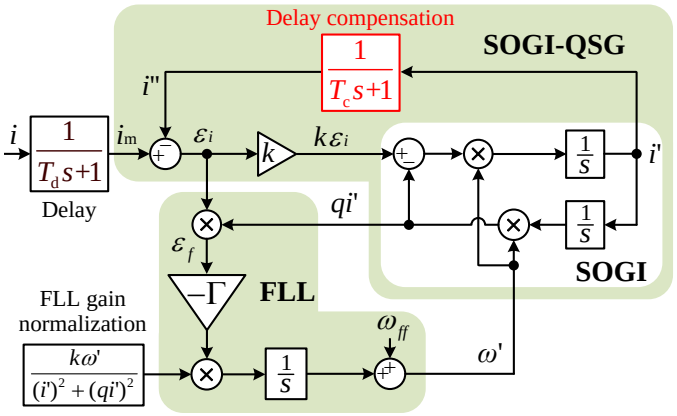

Fig. 7. Modified SOGI-FLL with the delay compensation.

The proposed delay compensation is implemented by inserting a first-order inertial term (actually a delay term) in the feedback path of SOGI-FLL. With the closed-loop control of SOGI-FLL, the infinite-gain of SOGI (at the resonance frequency) makes the delayed feedback signal track the fundamental component of the input signal with a zero steady-state error. Thus the output of SOGI-FLL can achieve a lead phase compared to the input signal, effectively compensating control and measurement delays. Similarly, the closed-loop structure for implementing the delay compensation is also adopted in the repetitive predictor [26], [31], which includes a delay term in the feedback path and has an infinite-gain controller.

In order to test the performance of the modified SOGI-FLL with the delay compensation, the output current of the converter

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i is structured as shown in (8), which contains a fundamental component i_1, 5th and 7th order harmonics, as well as the high-frequency *random noise* generated by the *band-limited white noise block* in MATLAB/Simulink.

$$i = 10\sin(\omega t) + 0.5\sin(5\omega t) + 0.2\sin(7\omega t) + random\ noise \quad (8)$$

The structured current i, the fundamental component i_1, and the the detected current i' by SOGI-FLL are shown in Fig. 8. As seen, the SOGI-FLL can effectively extra the fundamental component from the current i with harmonics and noise. However, without the delay compensation, the detected i' lags i_1 by T_d, which is set to be a relatively large value to make the delay clear. At 0.5s, after the delay compensation term $1/(T_c s+1)$ is added, the delay in i' is effectively compensated.

Note that, the harmonic attenuation performance of a single SOGI-FLL is limited, leading to the slight distortion in the detected i' as seen in Fig. 8. Nevertheless, the distortion will not seriously affect the zero-crossing point, thus the accuracy of the obtained current polarity can be guaranteed for the implementation of the dead-time elimination PWM. To further enhance the accuracy of the obtained current polarity, the multi-SOGI-FLL in [38] can be applied which however will increase the complexity of the system. Considering the total harmonic distortion (THD) of the converter output current is limited below 5% by IEEE standard 1547-2003 [39], a single SOGI-FLL can be adequate to accurately obtain the current polarity in practice.

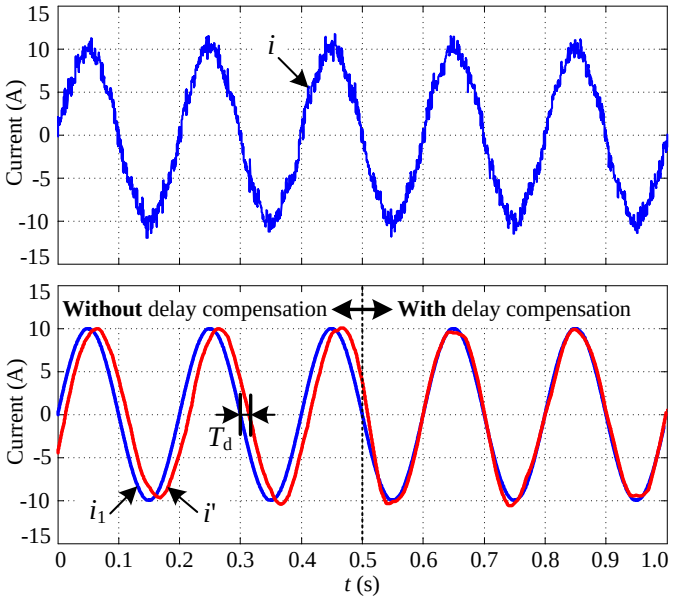

Fig. 8. Performance of the modified SOGI-FLL with the delay compensation.

V. Proposed DSOGI-FLL-based Dead-Time Elimination PWM

A. SOGI-FLL-based Dead-Time Elimination PWM

For the single-phase converter or the balanced three-phase converter, the dead-time elimination can be implemented based on the SOGI-FLL. For example, in the single-phase converter shown in Fig. 9, the voltage modulation wave u^* is used to compare with the triangle carrier generating the drive pulses. The current i' is detected by SOGI-FLL from the measured output current i_m of the converter. The polarity of i' is used to alternate the drive pulses of the dead-time elimination PWM. When $i'>0$, drive signals for Q_1^+ and Q_2^- are enabled, for Q_1^- and Q_2^+ disabled; otherwise, drive signals for Q_1^- and Q_2^+ are enabled, for Q_1^+ and Q_2^- disabled.

In the balanced three-phase converter shown in Fig. 10, voltage modulation waves u_a^*, u_b^*, and u_c^* are used to generate three-phase drive pulses. With the SOGI-FLL, i' and its in-quadrature signal qi' are obtained from one of the measured three-phase currents, e.g. i_{am}. Based on i' and qi', new three-phase current references i_a^*, i_b^*, and i_c^* are generated by the Clark inverse transformation whose current polarities are used for alternating the three-phase drive pulses in the dead-time elimination PWM. Taking Phase A for example, when $i_a^*>0$, the drive pulse for Q_a^+ will be enabled, for Q_a^- disabled; otherwise, the drive pulse for Q_a^- will be enabled, for Q_a^+ disabled. Similarly, the drive pulses for Q_b^+, Q_b^-, Q_c^+, and Q_c^- can be distributed according to the polarities of i_b^* and i_c^*, respectively.

However, the SOGI-FLL-based dead-time elimination PWM with one phase current measured can only be used in the three-phase converter with balanced currents where the phase difference among three-phase currents is strictly equal to $2\pi/3$. In the three-phase converter with faulty unbalanced currents, a single SOGI-FLL will be not suitable to detect current polarities for the dead-time elimination PWM anymore.

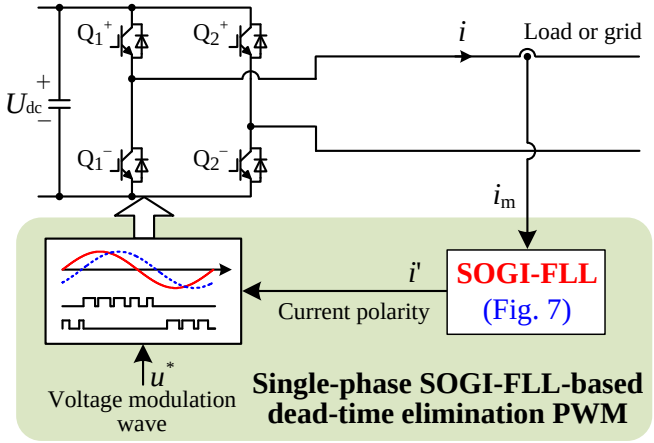

Fig. 9. Diagram of the SOGI-FLL-based dead-time elimination PWM for single-phase converters.

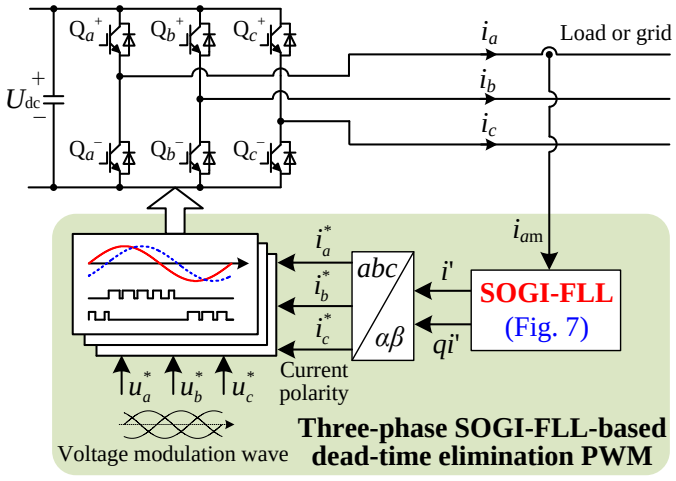

Fig. 10. Diagram of the SOGI-FLL-based dead-time elimination PWM for three-phase converters with balanced currents.

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B. Analysis of the Phase Difference between Unbalanced Currents

In three-phase three-wire power systems, neglecting the zero-sequence component, the unbalanced currents can be expressed as

$$\boldsymbol{i}_{abc} = \boldsymbol{i}^{\mathrm{p}}_{abc} + \boldsymbol{i}^{\mathrm{n}}_{abc} = I^{\mathrm{p}}\begin{bmatrix}\cos(\omega t+\varphi_{\mathrm{p}})\\ \cos(\omega t+\varphi_{\mathrm{p}}-2\pi/3)\\ \cos(\omega t+\varphi_{\mathrm{p}}-4\pi/3)\end{bmatrix} + I^{\mathrm{n}}\begin{bmatrix}\cos(\omega t+\varphi_{\mathrm{n}})\\ \cos(\omega t+\varphi_{\mathrm{n}}+2\pi/3)\\ \cos(\omega t+\varphi_{\mathrm{n}}+4\pi/3)\end{bmatrix} \tag{9}$$

where the scripts 'p' and 'n' respectively represent the positive- and negative-components. The unbalanced three-phase current vectors synthesized by the positive- and negative-components are illustrated in Fig. 11. As seen, the phase difference among the synthesized three-phase currents is not evenly equal to 2π/3, and the amplitude are not the same either.

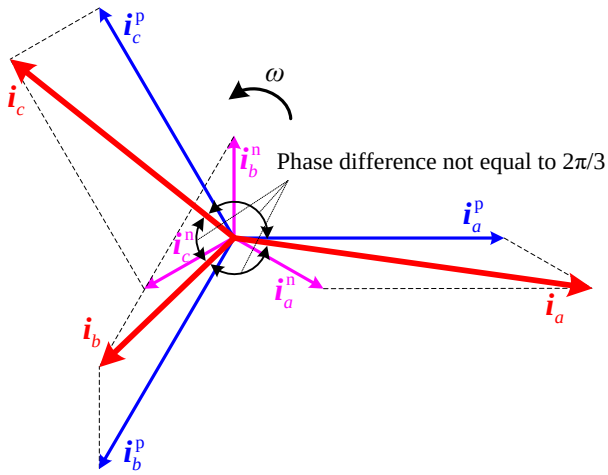

Fig. 11. Unbalanced current vectors synthesized by positive- and negative-components.

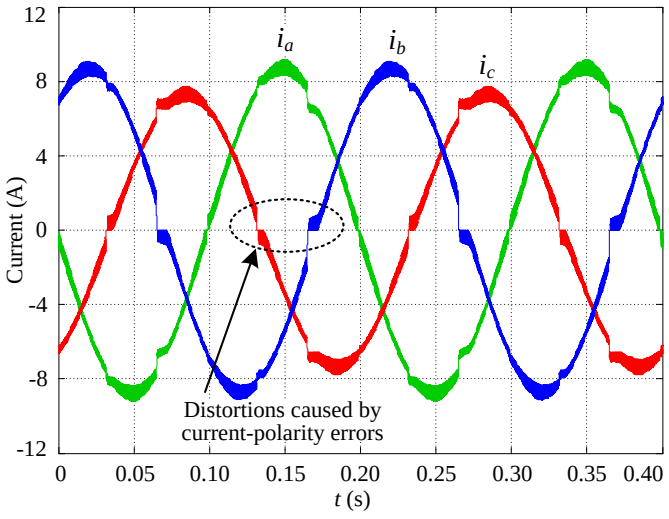

Fig. 12. Performance of the SOGI-FLL-based dead-time elimination PWM with unbalanced currents.

In the unbalanced current condition, if the SOGI-FLL-based dead-time elimination PWM in Fig. 10 is still adopted, only the current polarity of one phase would be accurate, and errors would exist in the polarities of the other two phase currents causing current distortions at corresponding zero-crossings. With the SOGI-FLL-based dead-time elimination PWM scheme in Fig. 10, the three-phase unbalanced output currents are obtained by simulation with unbalanced *RL* load as shown in Fig. 12. As seen, i_a has the minor distortion at zero-crossing, while serious distortions occur at zero-crossings of i_b and i_c. Besides, the zero-crossing distortions also deteriorate the waveforms the three-phase currents at the corresponding positions. In order to accurately detect the polarities of unbalanced currents, instead of using the SOGI-FLL, the DSOGI-FLL [23]-[25] can be adopted to track both the positive- and negative-sequence components, which will be introduced in next section.

C. DSOGI-FLL for the Unbalanced Current Condition

The structure of the DSOGI-FLL implemented in the $\alpha\beta$ frame is shown in Fig. 13. The input signals $i_{\alpha\mathrm{m}}$ and $i_{\beta\mathrm{m}}$ are calculated by the Clark transformation from the measured three-phase currents of the converter. Two SOGI-QSGs are respectively in charge of generating the direct and in-quadrature signals, i.e. i_α', i_β', qi_α', and qi_β'. These signals can be further used to calculate the positive-/negative-sequence components [25]. Due to the input signals $i_{\alpha\mathrm{m}}$ and $i_{\beta\mathrm{m}}$ have the same frequency, a single FLL is adopted to make the DSOGI become frequency adaptive. The average frequency error variable ε_f is calculated by $(\varepsilon_{f(\alpha)}+\varepsilon_{f(\beta)})/2$ as the input of the integration in FLL. In addition, the delay compensation term $1/(T_c s+1)$ is also inserted in the feedback paths of the two SOGI-QSGs to compensate the current measurement delay and the control delay. Based on the DSOGI-FLL, a new dead-time elimination PWM will be proposed in next section.

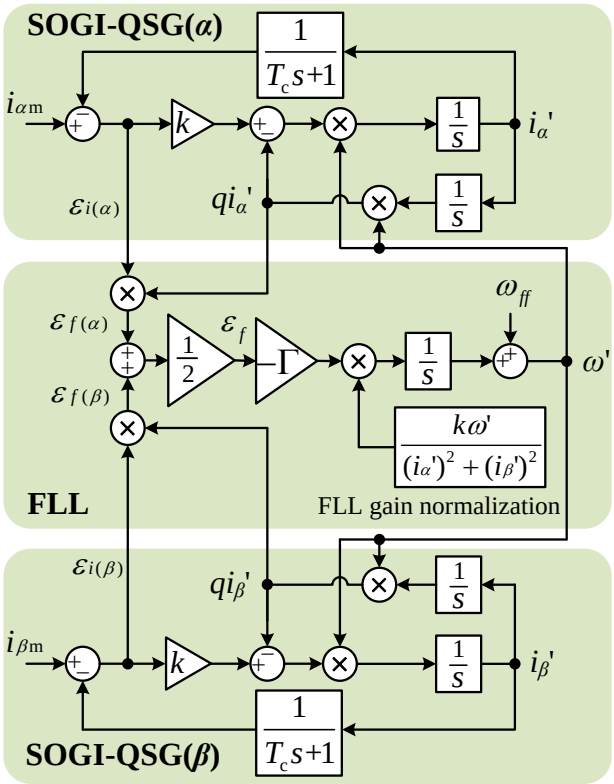

Fig. 13. Structure of the DSOGI-FLL with the delay compensation.

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D. Proposed DSOGI-FLL-based Dead-Time Elimination PWM

The proposed DSOGI-FLL-based dead-time elimination PWM is shown in Fig. 14. Voltage modulation waves u_a^*, u_b^*, and u_c^* are used to compare with the carrier generating three-phase drive pulses. In order to alternate the drive pulses implementing the dead-time elimination PWM, the three-phase load currents are measured and transferred to the $\alpha\beta$ frame ($i_{\alpha m}$ and $i_{\beta m}$) as the inputs of the DSOGI-FLL. Then, i_α' and i_β' are extracted, and transferred back to the *abc* frame as current references i_a^*, i_b^*, and i_c^*, which provide the current polarity information for distributing the drive pulses.

The performance of the DSOGI-FLL-based dead-time elimination PWM with unbalanced output currents are shown in Fig. 15. As seen, the zero-crossing distortions of all the three-phase currents are minimized compared to those in Fig. 12, due to the DSOGI-FLL can track both the positive- and negative-sequence components obtaining accurate polarities for all the three-phase currents.

Note that, due to the current references i_a^*, i_b^*, and i_c^* are calculated from the DSOGI-FLL outputs i_α' and i_β', it is unnecessary to respectively figure out the positive- and negative-sequence components in the implementation of DSOGI-FLL-based dead-time elimination PWM, so that the computation burden can be reduced.

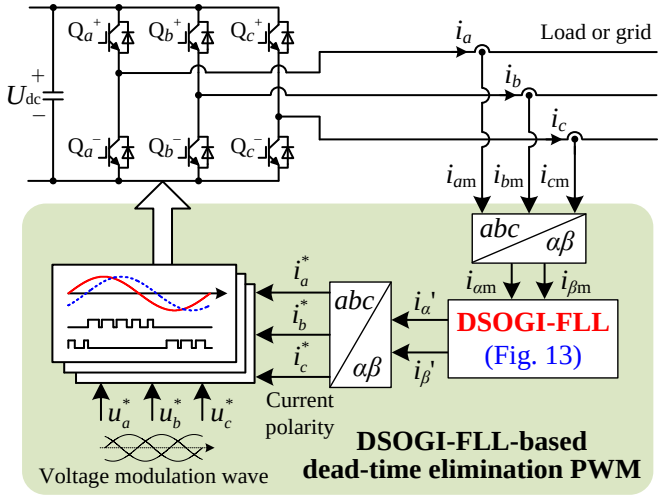

Fig. 14. Diagram of the DSOGI-FLL-based dead-time elimination PWM for three-phase converters with both unbalanced and balanced currents.

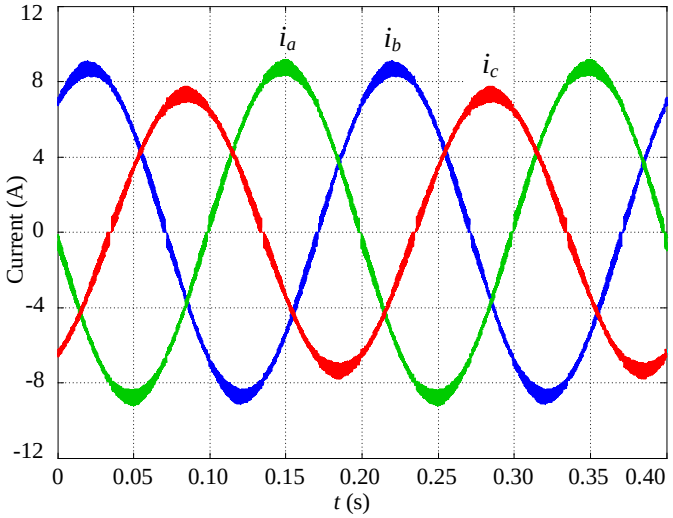

Fig. 15. Performance of the DSOGI-FLL-based dead-time elimination PWM with unbalanced currents.

VI. Application of the Dead-Time Elimination PWM in the Grid-Connected Converter

The proposed DSOGI-FLL-based dead-time elimination PWM can be applied to the existing control scheme conveniently. As an application example, it has been inserted into the commonly used feedforward decoupling scheme with PI controllers in the *dq* frame to control the grid-connected converter [40], as shown in Fig. 16. Voltage modulation waves u_a^*, u_b^*, and u_c^* for the DSOGI-FLL-based dead-time elimination PWM are regulated by the current loop. The measured three-phase currents i_{am}, i_{bm}, and i_{cm} are simultaneously used as the feedback of the current loop and the inputs of the DSOGI-FLL to obtain current polarities for the dead-time elimination PWM. And the angle θ of the grid voltage is obtained by a phase-locked loop (PLL) [41] to implement the grid-voltage oriented vector control.

In the scheme shown in Fig. 16, the input currents i_{am}, i_{bm}, and i_{cm} of the DSOGI-FLL-based dead-time elimination PWM are only used for obtaining the current polarities, which is not an extra current control loop. Therefore, the stability performance of the current loop will not be influenced by the inserted DSOGI-FLL-based dead-time elimination PWM, even though turbulences may be generated at current zero-crossings when alternate the upper and the lower drive pulse. The scheme show in Fig. 16 will be finally validated by grid-connected experiments.

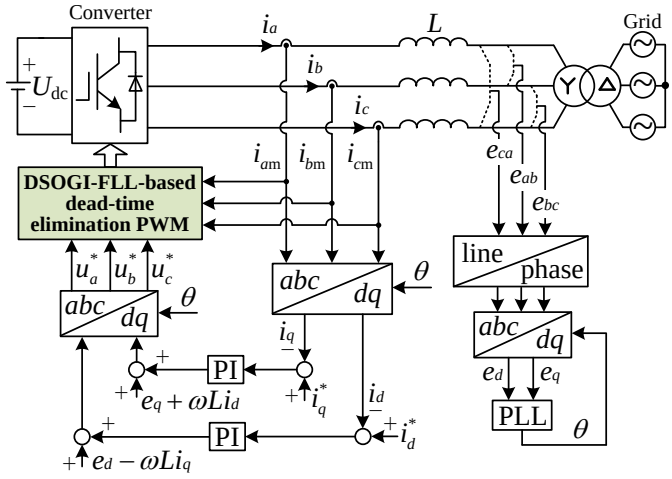

Fig. 16. Application of the DSOGI-FLL-based dead-time elimination PWM in the grid-connected converter.

VII. Experimental Test and Results

The performance of the proposed DSOGI-FLL-based dead-time elimination PWM is tested on a three-phase converter experimental setup as shown in Fig. 17. Experiments are first carried out with an adjustable *RL* load for the convenient of testing dynamic performances in unbalanced-current, power-change, and frequency-variation conditions. Afterwards, the DSOGI-FLL-based dead-time elimination PWM is further implemented in the grid-connected condition through a transformer to verify its feasibility in practical applications. The dc-link voltage is supplied by the Chroma programmable dc power supply 62050H-600S. The TI DSP TMS320F28335 and ALTERA CPLD EPM240T100 are adopted on the control board to implement the control strategies. Experimental waveforms are captured by the HDO4024 200MHz 2.5GS/s oscilloscope from Teledyne LeCroy. Parameters of the test system are given in Table I.

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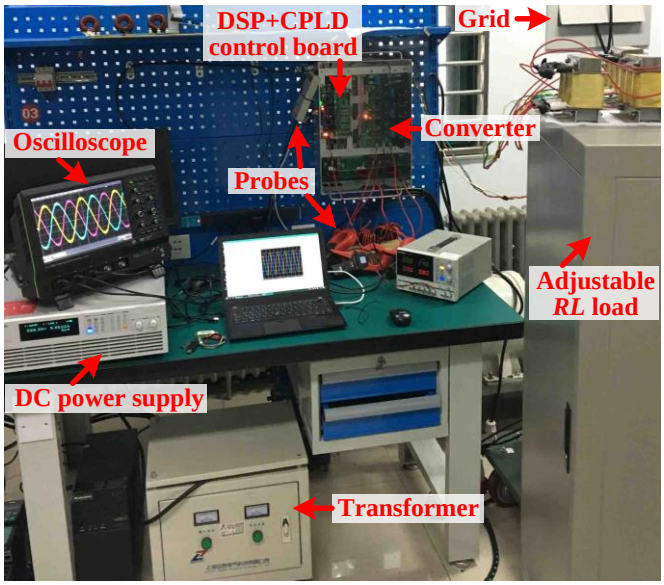

Fig. 17. Experimental setup of the three-phase converter.

TABLE I
PARAMETERS OF THE TEST SYSTEM

Symbol	Parameter	Value
S	Rated capacity	10kVA
U_{dc}	DC-link voltage	600V
f_s	Switching frequency	20kHz
M	Modulation index	0.8
L_{load}	Load inductance of each phase	4.2mH
R_{BL}	Balanced load resistance of each phase	27Ω
R_{UL}	Unbalanced three-phase load resistances	27Ω, 27Ω, 37Ω
L	Inductance of the L filter	3.8mH
η	Transformer voltage ratio	380V / 304V

The scheme of the DSOGI-FLL-based dead-time elimination PWM shown in Fig. 14 is adopted in the experiments with the adjustable *RL* load. Fig. 18 shows the reference current i_a^* outputted by a digital-to-analog converter (DAC), as well as the drive pulses S_a^+ and S_a^- enabled alternately according to the polarity of i_a^*. As seen from the zoomed-in detail of the 20kHz drive pulses, an underlap period which equals to two switching periods has been added when alternating the drive pulses to smooth the current jump at the zero-crossing.

In order to verify the effectiveness of the added underlap period in drive pulses and the delay compensation in DSOGI-FLL respectively proposed in Section III and IV-B, experiments are carried out with different strategies. The corresponding three-phase currents and the zoomed-in zero-crossings are shown in Fig. 19, Fig. 20, and Fig. 21, respectively.

In Fig. 19, the DSOGI-FLL-based dead-time elimination PWM without the delay compensation is adopted, and an underlap period equal to two switching periods has been added when alternating the drive pulses. As seen in Fig. 19(a), obvious distortions appear at the zero-crossings of the three-phase currents. The zoomed-in current zero-crossing is shown in Fig. 19(b), where $\overline{i_c}$ is the mean value of i_c computed over a running average window of one switching cycle, and a bias of 1.3A has been added for a clear display. The current zero-crossing is delayed about 150μs, which contains the current measurement delay (about 100μs) and the control delay (50μs for 20kHz). With the delayed zero-crossing, distortions are thus generated in the three-phase currents.

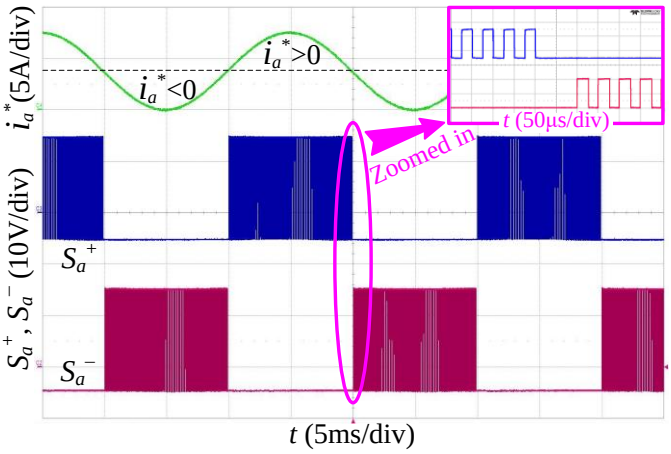

Fig. 18. Waveforms of the current reference i_a^* and the drive pulses S_a^+ and S_a^- with an underlap period at the zero-crossing.

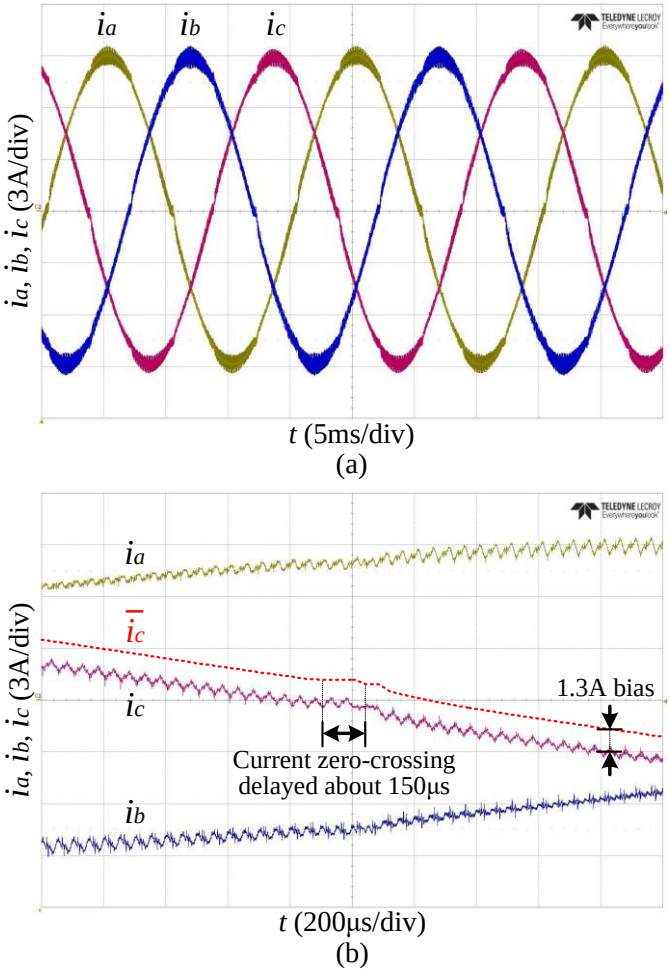

Fig. 19. Experimental results of the DSOGI-FLL-based dead-time elimination PWM **without** the delay compensation while **with** the underlap period in drive pulses: (a) three-phase currents and (b) the zoomed-in zero-crossing.

To mitigate the zero-crossing distortion, the delay compensation with T_c=150μs is employed in the DSOGI-FLL-based dead-time elimination PWM, while the underlap period when alternating the drive pulses is not applied. Consequently, the current zero-crossing distortions in Fig. 20(a) have been reduced compared with those in Fig. 19(a). However as shown in Fig. 20(b), the current jump at the zero-crossing can still be a reason causing the current distortion.

Afterwards, both the delay compensation and the underlap period equal to two switching periods are employed in the

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DSOGI-FLL-based dead-time elimination PWM. Fig. 21(a) shows the corresponding three-phase currents with further improved current zero-crossings. In Fig. 21(b), instead of the current jump, a flat current segment is generated by the underlap period in drive pulses helping the current cross zero smoothly.

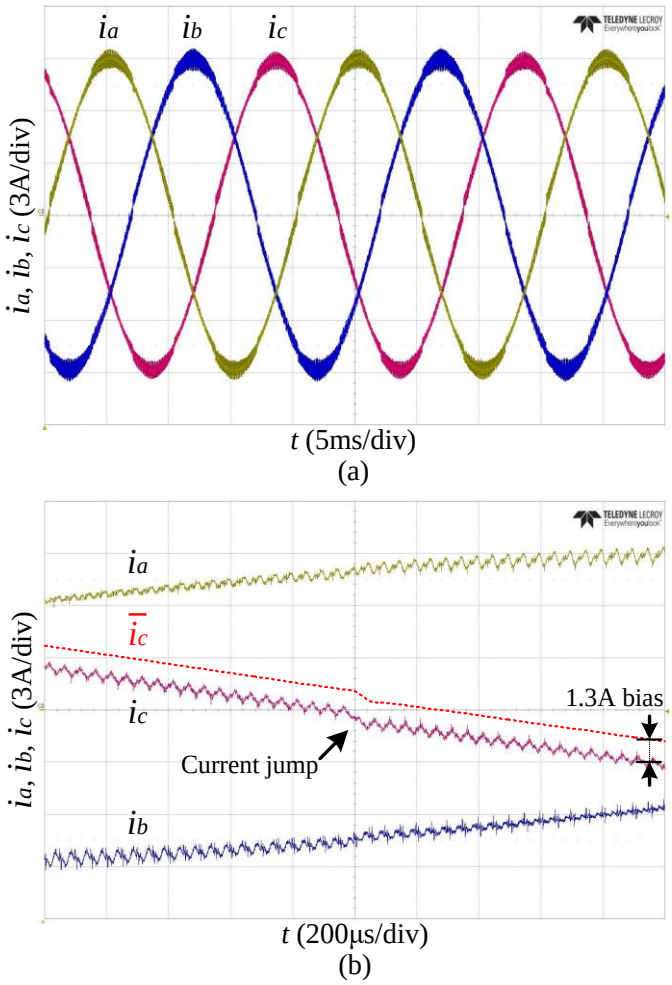

Fig. 20. Experimental results of the DSOGI-FLL-based dead-time elimination PWM **with** the delay compensation while **without** the underlap period in drive pulses: (a) three-phase currents and (b) the zoomed-in zero-crossing.

As a comparison, an experiment is further carried out using the conventional PWM with the dead-time of 1.8μs. The captured three-phase currents are presented in Fig. 22. And Fig. 23 shows the fast Fourier transformation (FFT) result and THD of the Phase A current respectively using the conventional PWM and the DSOGI-FLL-based dead-time elimination PWM. The THD is computed up to 100kHz. As seen, the odd harmonics and THD with the dead-time elimination PWM are all lower than those with the conventional PWM. However, due to the dead-time elimination PWM can generate the current zero-crossing distortion though not obvious, the even harmonics are relatively larger than those with the conventional PWM. In addition, with the same experimental parameters, the fundamental current in Fig. 21(a) is larger than that in Fig. 22, 8.94A and 7.82A (Phase A) respectively, which can indicate the dead-time elimination PWM has a larger dc-link voltage utilization compared with the conventional PWM.

Three-phase load resistances of 27Ω, 27Ω, and 37Ω are employed to test the performance of the dead-time elimination PWMs respectively based on SOGI-FLL and DSOGI-FLL in the unbalanced current condition. As seen the captured currents in Fig. 24, the SOGI-FLL-based dead-time elimination PWM scheme in Fig. 10 is first adopted, serious distortions appear at the current zero-crossings of Phase B and C, due to the phase difference among the unbalanced three-phase currents is not evenly equal to 2π/3. After the DSOGI-FLL-based dead-time elimination PWM is applied, the zero-crossing distortions of all the three-phase currents are mitigated, proving a good adaptability for the unbalanced current condition.

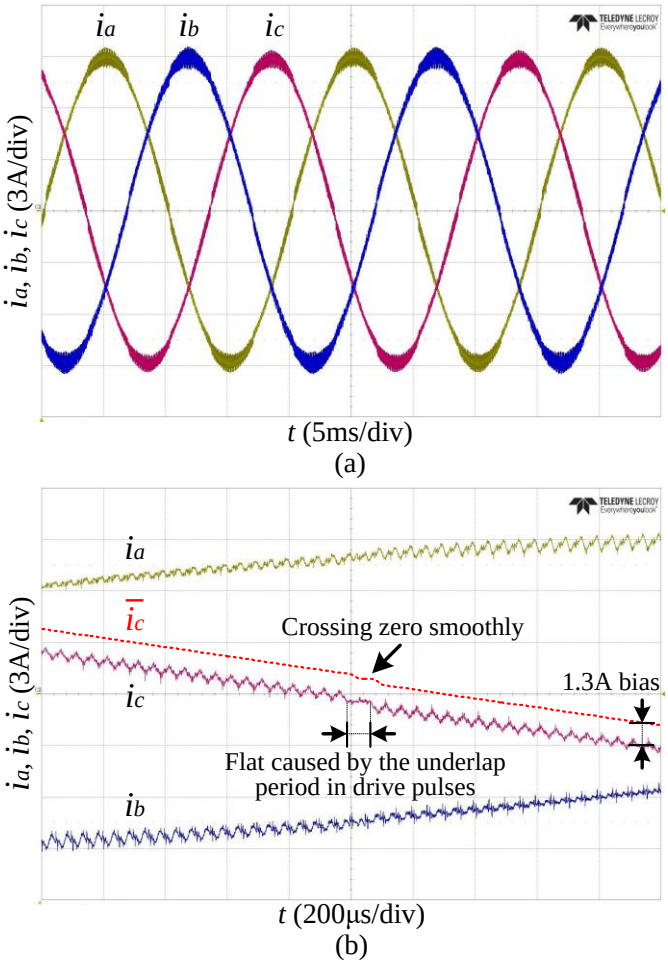

Fig. 21. Experimental results of the DSOGI-FLL-based dead-time elimination PWM **with both** the delay compensation and the underlap period in drive pulses: (a) three-phase currents and (b) the zoomed-in zero-crossing.

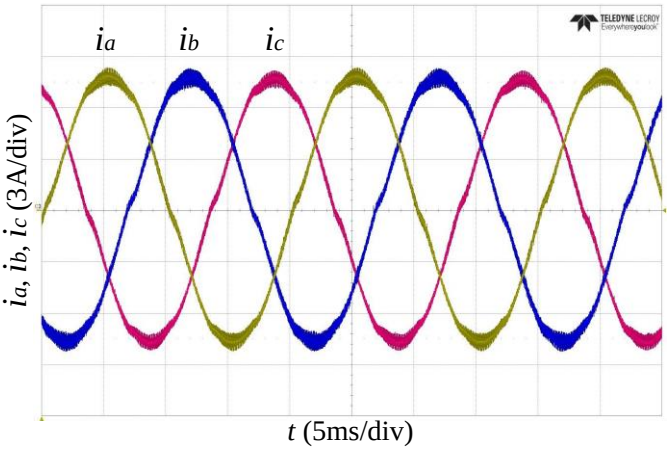

Fig. 22. Three-phase currents with the dead-time of 1.8μs.

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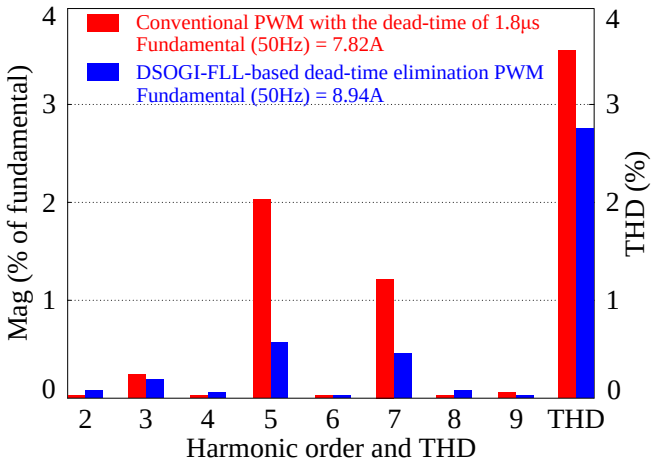

Fig. 23. FFT results and THD of the Phase A current respectively using the conventional PWM with the dead-time of 1.8μs and the DSOGI-FLL-based dead-time elimination PWM.

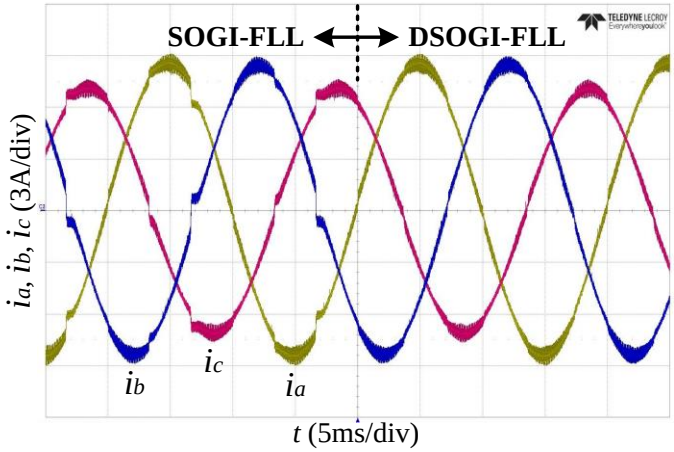

Fig. 24. Performance of the SOGI-FLL-based and the DSOGI-FLL-based dead-time elimination PWMs in the unbalanced current condition.

Fig. 25 shows the dynamic three-phase currents with the operating power increased from 1923W to 3330W. During the power increasing process, neither distortion nor overshoot appear in the currents. It can be indicated that, the proposed DSOGI-FLL-based dead-time elimination PWM can work well in the power-variation condition.

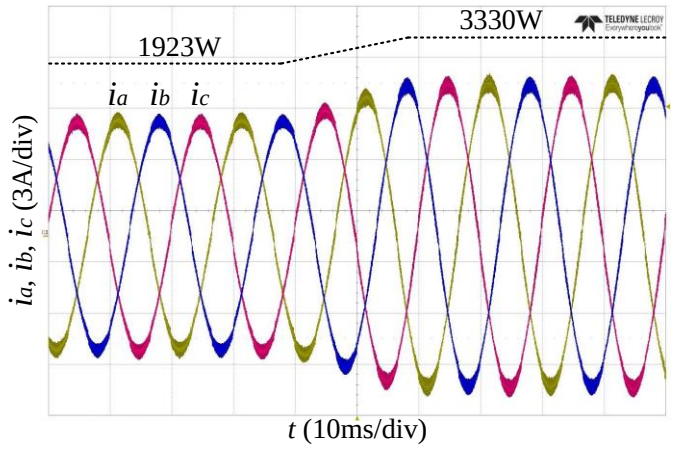

Fig. 25. Dynamic three-phase currents with the operating power increased from 1923W to 3330W.

The frequency adaptability of the DSOGI-FLL-based dead-time elimination PWM is tested respectively with different frequency-increasing steps as seen in Fig. 26, where the current frequency ω' is obtained by the DSOGI-FLL and outputted by a DAC. In Fig. 26(a), the current frequency is increased from 80π rad/s (40Hz) to 100π rad/s (50Hz). During the frequency increasing process, current distortions appear in the three-phase currents, which can be acceptable due to the current shape still remains sinusoidal. However, in Fig. 26(b) where the current frequency is increased from 60π rad/s (30Hz) to 100π rad/s (50Hz), much more serious distortions are generated in the currents. The reason is that, the faster the current frequency increases, the larger the tracking error will exist in ω' as well as in the current polarity obtained by the DSOGI-FLL, thus causing more serious current distortions. Therefore, in the application of the DSOGI-FLL-based dead-time elimination PWM, a sudden change of the current frequency should be avoided in case of causing the system instability.

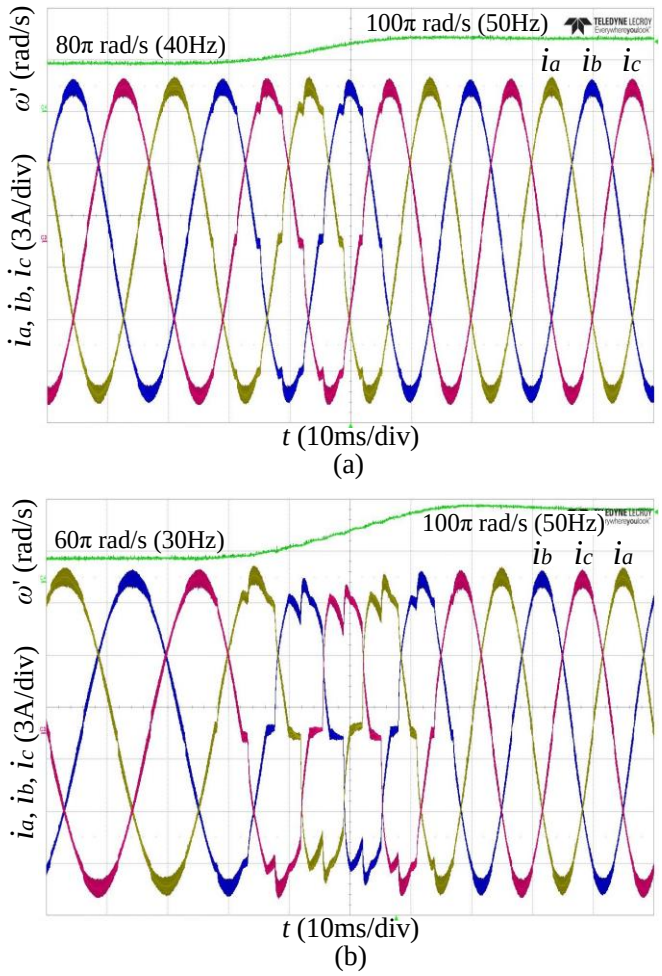

Fig. 26. Frequency adaptability test of the DSOGI-FLL-based dead-time elimination PWM: (a) with the current frequency increasing from 80π rad/s to 100π rad/s and (b) with the current frequency increasing from 60π rad/s to 100π rad/s.

To verify the feasibility in practical applications, the proposed DSOGI-FLL-based dead-time elimination PWM is applied to the converter connected to the grid through a transformer with the scheme shown in Fig. 16. Fig. 27 shows the three-phase currents and the Phase A grid voltage with a unity power factor. The operating power is 4312W. The THDs of three-phase currents computed up to 100kHz are 3.62%, 3.71%, 3.81%, respectively, which can well meet the limit of 5% defined by IEEE Standard 1547-2003 [39].

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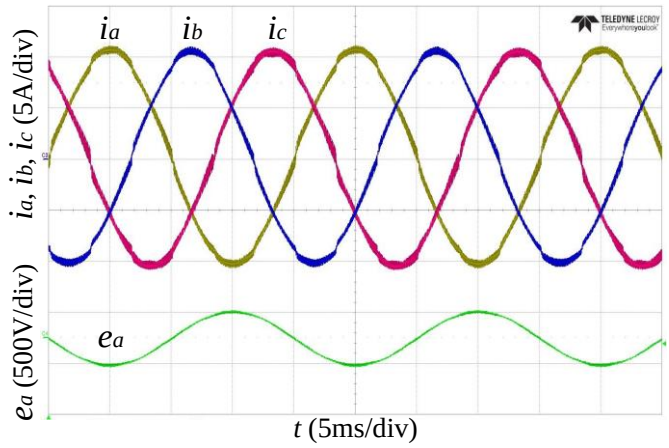

Fig. 27. Three-phase currents and the Phase A grid voltage.

To further discuss the application of the proposed DSOGI-FLL-based dead-time elimination PWM, converters are grouped into two categories: a) conventional converters for transferring the active/reactive power and b) active power filters specially for generating current harmonics [42], based on which discussions are given as follows.

a) Regarding conventional converters, e.g. photovoltaic inverters and motor-drive converters, the output current is mainly composed of a fundamental current and a small quantity of current harmonics. With the THD requirement below 5%, the polarity of fundamental current can be taken as the polarity of the whole output current regardless of the influence of current harmonics. Therefore in conventional converters, with the DSOGI-FLL or the multi-SOGI-FLL [38], accurate current polarities can be obtained making the dead-time elimination PWM work well.

b) The active power filter is used for compensating current harmonics caused by nonlinear loads. Therefore, the output current of active power filter is composed of current harmonics with the same amplitude but opposite phase angle [42]. With a large quantity of current harmonics, using the DSOGI-FLL or even the multi-SOGI-FLL [38], it is still hard to accurately obtain the polarity of the output current with random zero-crossings. Given the implementation of the dead-time elimination PWM is on the premise of knowing the current polarity, the proposed DSOGI-FLL-based dead-time elimination PWM cannot work well or even is not applicable in active power filters.

VIII. Conclusion

A DSOGI-FLL-based dead-time elimination PWM has been proposed for the three-phase converter in this paper. An underlap period has been added when alternating the upper and the lower drive pluses to smooth the current jump at zero-crossing. And the delay compensation term has been inserted in the DSOGI-FLL to compensate both the current measurement delay and the control delay. Compared with the conventional PWM with dead-time, odd current harmonics can be effectively reduced, while even harmonics will be slightly increased due to the drive pulse alternation. The proposed DSOGI-FLL-based dead-time elimination PWM can work well in the unbalanced-current and power-change conditions, while the sudden current-frequency change should be avoided in case of system instability. The DSOGI-FLL-based dead-time elimination PWM can be inserted into the existing control scheme conveniently, e.g. the commonly used feedforward decoupling scheme with PI controllers in the *dq* frame for grid-connected converters.

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